UNITED STATES PATENT AND TRADEMARK OFFICE

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10/697,503	10/30/2003	David A. Luick	ROC920020009US1	8053

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *16 October 2007*.

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *2-8,10-14,17 and 19* is/are pending in the application.

   4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *2-8,10-14,17 and 19* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/ are: a) ☐ accepted or b) ☐ objected to by the Examiner.

   Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

   Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   a) ☐ All b) ☐ Some * c) ☐ None of:

   1. ☐ Certified copies of the priority documents have been received.

   2. ☐ Certified copies of the priority documents have been received in Application No. _____.

   3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the applicant's submission of the RCE dated 10/16/2007. At this point claims 2-8, 10-14, 17 and 19 are pending in the instant application.

Response to Amendment

In view of the affidavit dated 7/26/2007, the 35 USC 103 rejection dated 7/16/2007 is withdrawn. The examiner directs the applicant's attention to the following new ground(s) of rejection.

Claim Objections

Claims 10-14 depend on now cancelled claim 18. The examiner requests the applicant to correct the matter. The examiner interprets that claims 10-14 depend on claim 17.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1.   Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by Chiarot et al.

(US 5,721,864).

2.   **Independent claim 19** discloses; "loading a speculative load **[prefetching to L1**

cache, Abstract] into the pipeline **[L1 & L2 cache, Figure 1]**",

"loading a non-speculative load into the pipeline **[prefetching to L2 cache, Step 240,**

Figure 2] a predetermined number of cycles after the action of loading a speculative

load **[after determining that the L1 speculative load is a miss, "L1 Miss on Line**

M", Figure 2]", and

"if the speculative load was a misprediction **["L1 Miss on Line M", Figure 2]**, then

invalidating the speculative load in the pipeline **[not accessing the speculative load in**

L1 cache, Figure 2] and executing the non-speculative load **[executing the L2 load,**

Step 205 & 206, Figure 2], otherwise executing the speculative load and invalidating

the non-speculative load **[executing the L1 load, Abstract]**".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

1.   Claims 2-6, 10-14 and 17 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Chiarot et al. (US 5,721,864) in view of Chiarot et al. (US 5,721,864)

and Au (US 5,548,795).

2.   As per **independent claim 17 & dependent claims 2 and 10**, Chiarot et al.

disclose; "a computer architecture able to selectively load **[prefetching to L1 cache,**

Abstract], execute **[instruction that initiates the prefetch, Abstract]** and flush

[cancel instructions, Column 4, Lines 66-67] a series of instructions",

"at least one fast-load cache that loads at least one speculative data load **[prefetching**

to L1 cache, Abstract] relative to the speculative instruction **[instruction that initiates**

the prefetch, Abstract]",

"at least one L1 data cache that loads at least one non-speculative data load

[prefetching to L2 cache, Step 240, Figure 2], corresponding to the speculative

instruction **[instruction that initiates the prefetch, Figure 2]** a predetermined number

of cycles after the fast-data cache loads the speculative load **[after determining that**

the L1 speculative load is a miss, "L1 Miss on Line M", Figure 2]",

"a circuit that determines if the speculative data load is a misprediction; and a circuit that

causes: if the speculative load is a misprediction **["L1 Miss on Line M", Figure 2]**,

inhibit execution of the speculative load **[not accessing the speculative load in L1 cache, Figure 2]** and execute the non-speculative load **[executing the L2 load, Step 205 & 206, Figure 2]**; and if the speculative load is not a misprediction, execute the speculative load **[executing the L1 load, Abstract]** and inhibit the non-speculative load".

Chiarot et al. do not disclose expressly that the computer architecture is implemented with "a pipeline".

Chiarot et al. disclose the "deeper pipelines" (Column 1, Lines 33-35) in the admitted prior arts section.

Chiarot et al. and Chiarot et al. are analogous art because they are from the same filed of endeavor of microprocessor systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Chiarot et al. by including pipelines in the system as taught by Chiarot et al. in column 1, at lines 33-35.

The motivation for doing so would have been "to improve the performance of processing systems" as expressly taught by Chiarot et al. in column 1, at lines 35-36.

Therefore, it would have been obvious to combine Chiarot et al. with Chiarot et al. for the benefit of faster processing system to obtain the invention as specified in claim 17.

Chiarot et al. do not disclose expressly flagging each of the series of instructions

to indicate dependence and executing/inhibiting the dependent instructions.

Au discloses "The D_Flag fields 308 in each record 202 indicate

dependency relative to a more forward command record 202" in column 8, at

lines 44-46 and in Figure 3. The dependent commands are executed/inhibited in

predetermined order (Abstract).

Chiarot et al. and Au are analogous art because they are from the same filed of

endeavor of processing instructions in a computer system.

At the time of the invention it would have been obvious to a person of ordinary

skill in the art to modify Chiarot by executing dependent commands according to the

command queue reordering process as taught by Au in the abstract.

The motivation for doing so would have been to process commands in a time and

computationally efficient manner as expressly taught by Au in the abstract.

Therefore, it would have been obvious to combine Au with Chiarot et al. for the

benefit of processing optimization to obtain the invention as specified in claim 17.

3.   **Claims 3 and 11** disclose, "one or more data loads in the pipeline are not

dependent on any specific data and not selectively flagged". **Au discloses "The**

D_Flag fields 308 in each record 202 indicate dependency relative to a more

forward command record 202" in column 8, at lines 44-46 and in Figure 3. Thus, the very first command is deemed to be independent and not flagged.

4.   **Claims 4 and 12** disclose, "the flag bit is within the instruction". Au discloses, in Figure 3, the "D_Flag" field 308 within "Command Record" 202. Record 202 corresponds to the "instruction" from the claim. The "D_Flag" is a bit since it represents a bistate field **(Column 7, Lines 46-48).**

5.   **Claims 5 and 13** disclose, "the flag is attached to the instruction". Au discloses, in **Figure 3,** the "D_Flag" field 308 attached to the "Logical Block Address" 302 and 304. The "Logical Block Addresses" correspond to the "data load" from the claim. In addition, examiner notes that mere separation of parts (i.e. flags and data load) is not a patentable distinction over the prior art. See MPEP 2144.04 (C).

6.   **Claims 6 and 14** disclose, "each flagged instruction is flushed **[cancel instructions, Column 4, Lines 66-67]** from the pipeline upon the determination of a misprediction for a data load **["L1 Miss on Line M", Figure 2]".**

7.   Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiarot et al. (US 5,721,864) in view of Chiarot et al. (US 5,721,864) and Au (US 5,548,795) as applied to claim 17 above, and further in view of "The Cache Memory Book" by Jim Handy.

8.   As per **claim 7**, Chiarot et al. and Au disclose the system recited in claim 17.

Chiarot et al. and Au do not disclose expressly, "a directory".

In paragraph 27 of the Applicant's specification, it is disclosed that a directory

can be omitted if the cache is a one-way associate or direct-map cache. **Handy**

discloses a two-way associative cache in Page 54, at lines 23-25. Since the cache

is not a one-way associate or direct-map cache, it inherently includes a directory.

Chiarot et al., Au and Handy are analogous art because they are from the same

field of endeavor of computer storage access/management.

At the time of the invention it would have been obvious to a person of ordinary

skill in the art to modify Chiarot et al. and Au by including the two-way associative cache

as taught by Handy in Page 54.

The motivation for doing so would have been the high hit rate of the small size

two-way associative cache as expressly taught by Handy in Page 55, Figure 2.9.

Therefore, it would have been obvious to combine Chiarot et al. and Au with

Handy for the benefit of high cache hit rate to obtain the invention as specified in claim

7.

9.   Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiarot et

al. (US 5,721,864) in view of Chiarot et al. (US 5,721,864) and Au (US 5,548,795) as

applied to claim 17 above, and further in view of Sato et al. (US 4,628,450).

10.   As per **claim 8**, Chiarot et al. and Au disclose the system recited in claim 17.

Chiarot et al. and Au do not disclose expressly that the cache "does not include a

directory".

Sato et al. discloses **"A set of routines which are frequently used in an OS is

stored in a local memory arranged in a CPU and having high-speed elements"** in

column 2, at lines 23-26, wherein the "local memory" corresponds to the "fast-load

data cache" from the claim. Sato et al. also discloses **"A local memory which has

part of address locations of the main memory as its address location, which is

accessed by a CPU, and which can obtain same effect as cache memory without

having cache directory"** in the Abstract.

Chiarot et al., Au and Sato et al. are analogous art because they are from the

same field of endeavor of computer storage access/management.

At the time of the invention it would have been obvious to a person of ordinary

skill in the art to modify Chiarot et al. and Au by including the high-speed "local memory"

without cache directory as taught by Sato et al. in column 2, at lines 23-26 and in the Abstract.

The motivation for doing so would have been the improved bus performance as expressly taught by Sato et al. in column 2, at lines 27-30.

Therefore, it would have been obvious to combine Chiarot et al. and Au with Sato for the benefit of improved bus performance to obtain the invention as specified in claim 8.

Conclusion

A.   Claims Rejected in the Application

Claims 2-8, 10-14, 17 and 19 have received a first action of the merits and are subject of a first action non-final.

B.   Direction of Future Remarks

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133.

If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published

applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For

more information about the PAIR system, see http://pair-direct.uspto.gov. Should you

have questions on access to the Private PAIR system, contact the Electronic Business

Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call

800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 5, 2008   Jae Un Yu

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